Self Introduction

- Education
  - Bachelor, the University of Aizu, 1998
  - Master, the University of Aizu, 2000
    - Prof. Marakhovsky was one of my supervisors
  - Ph.D, the University of Tokyo, 2003
- Employment
  - Research associate, the University of Tokyo, 2004
  - Assistant professor, the University of Aizu, 2005 – current
- Research interests
  - Design automation for asynchronous circuits and design automation for network-on-chip

Self Introduction

- Teaching
  - Undergraduate school
    - Two courses related to logic circuit designs
  - Graduate school
    - Two courses related to design automation of VLSIs
    - One seminar course
- Lab
  - Supervising 14 students
    - 1 Ph.D student
    - 8 master students
    - 5 bachelor students

MY COURSES

Hiroshi Saito
Assistant Professor
The University of Aizu
hiroshis@u-aizu.ac.jp

Undergraduate school

- Logic circuit design
  - Lecture: Boolean algebra, truth table, synthesis of logic functions, FSM design, etc
  - Exercise: Schematic design and simulation
- Advanced logic circuit design
  - Lecture: Verilog HDL, logic synthesis, etc
  - Exercise: Design of simple circuits using Altera FPGA

Graduate school

- CADI
  - From Verilog RTL model to Layout design through logic synthesis and layout verification
  - It will be rearranged to design something using Cadence tools
- CADII
  - From SystemC functional model to Verilog RTL model through SystemC, transaction-level modeling, and behavioral synthesis
  - It will also be rearranged to design something using Cadence tools
- Creative factory seminar
  - SoC design using Altera FPGA and Nios II

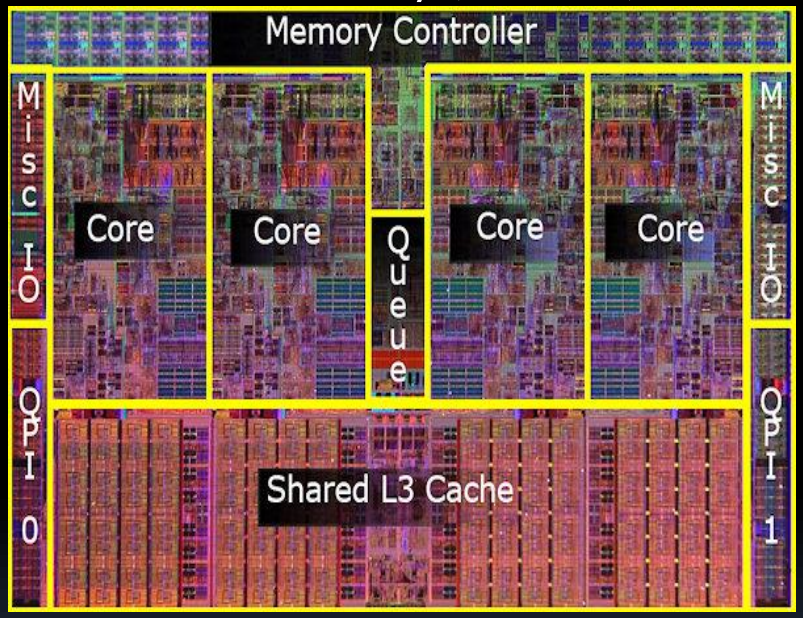
DESIGN AUTOMATION FOR ASYNCHRONOUS CIRCUITS

Hiroshi Saito
Assistant Professor
The University of Aizu
hiroshis@u-aizu.ac.jp

VLSI Integration Technologies

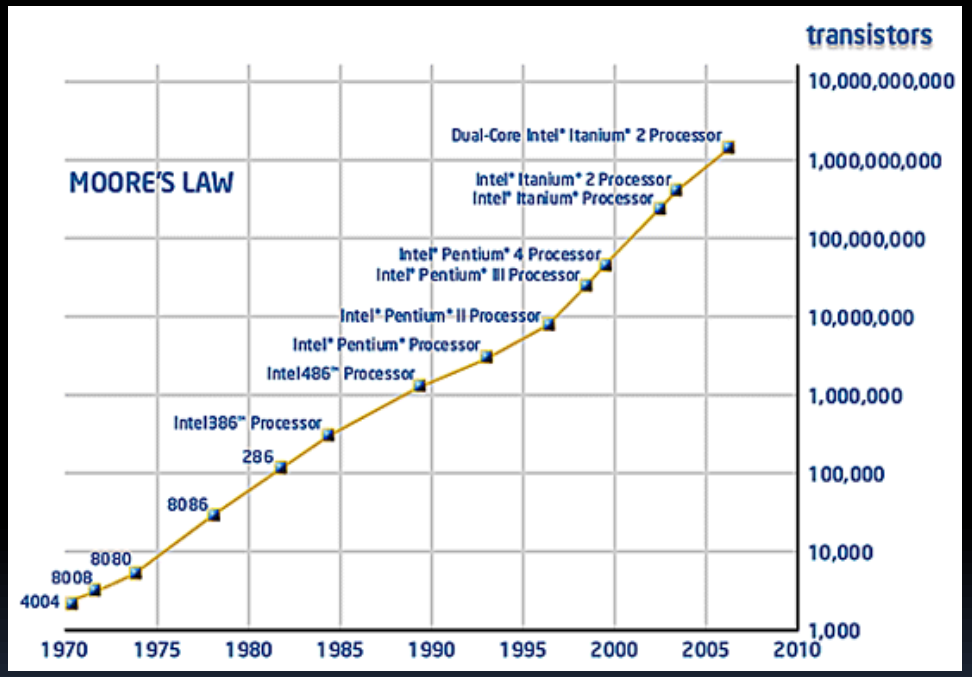
- Advance of deep sub-micron technology
  - Shrinking down of transistor size

Intel Core i7 (2008～)



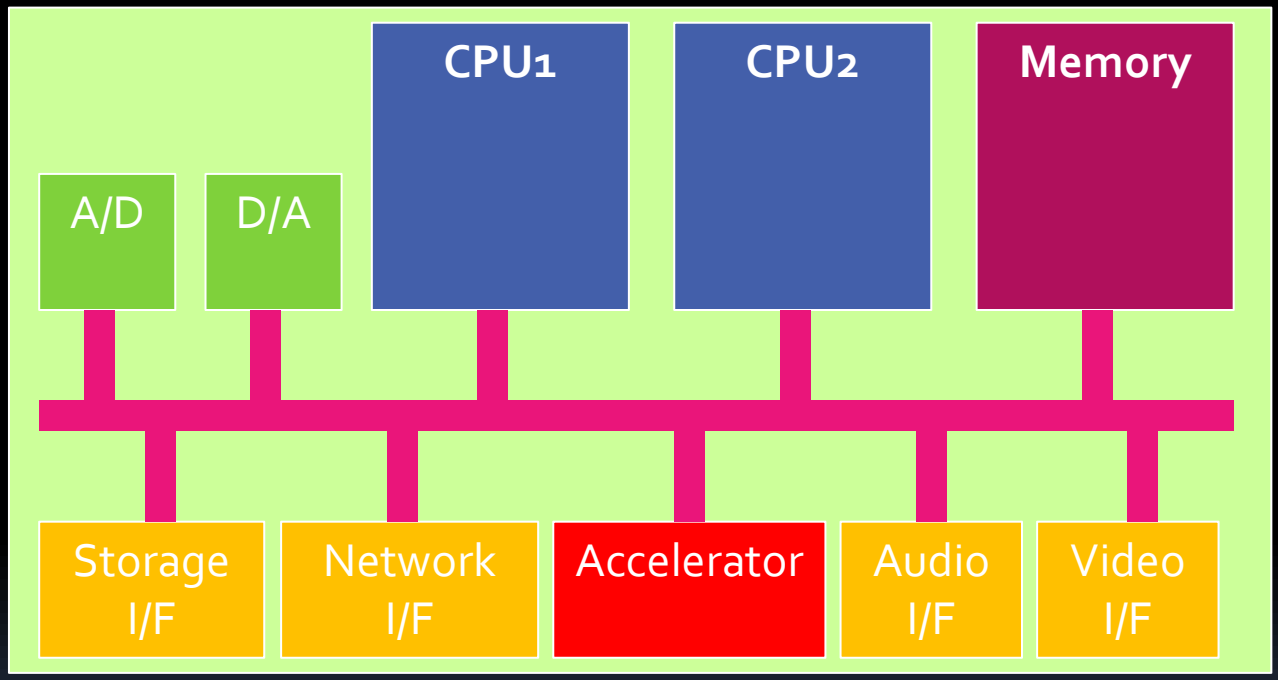
774,000,000 transistors
1.06 – 3.40 GHz

Moore's law



System-on-Chip

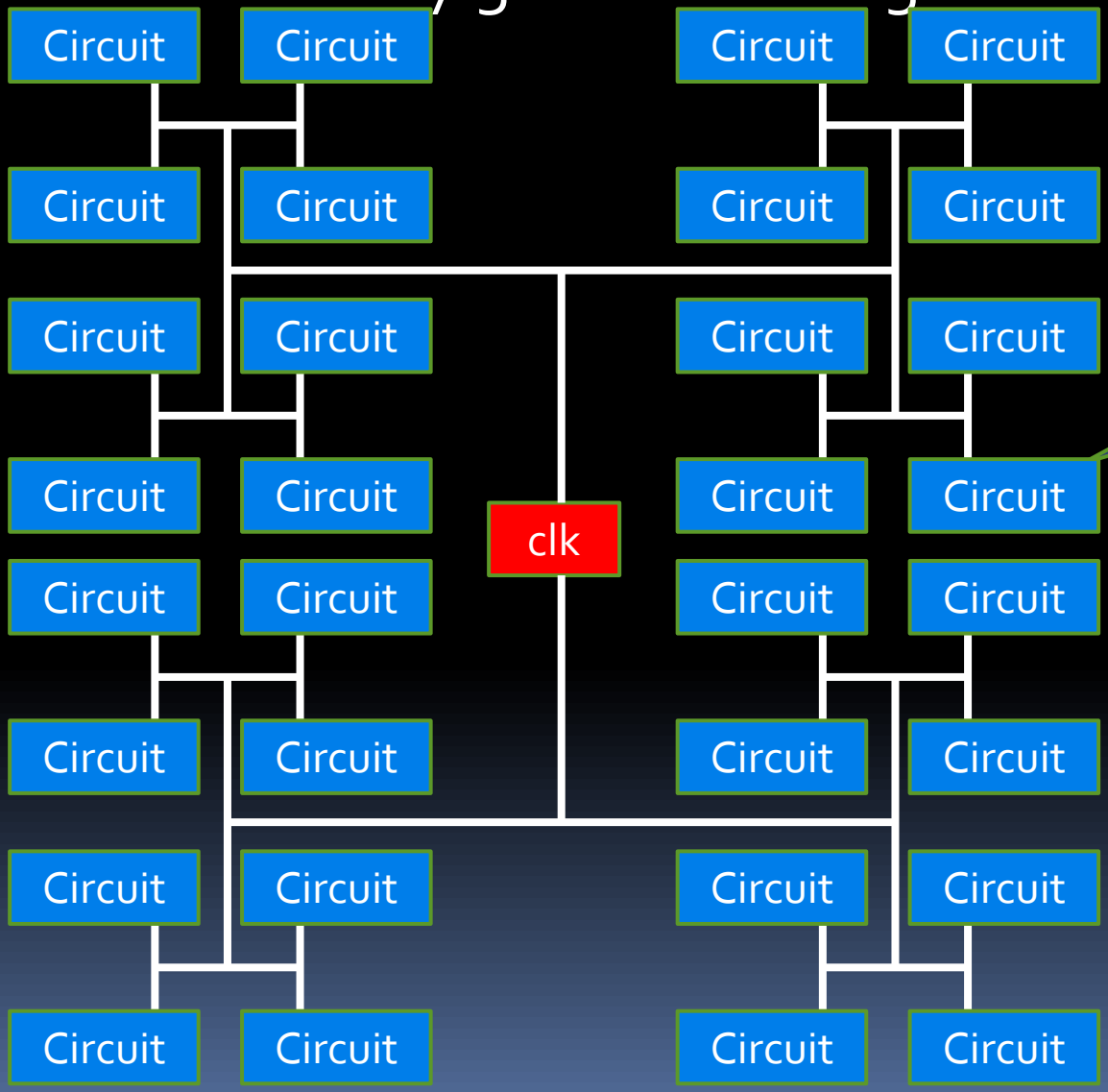
- A computer system is realized on a chip
  - Multi-core/many-core system

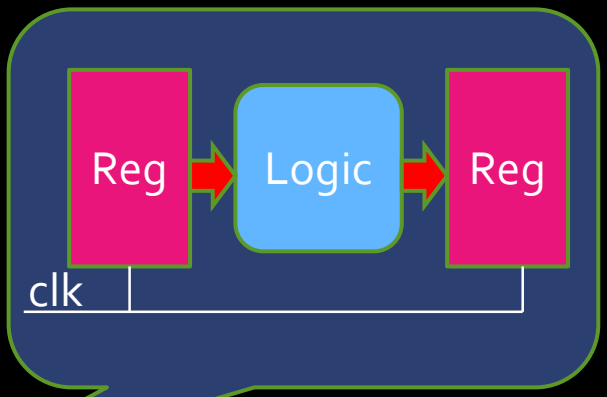


Hardware & software → Digital & analog → Electronics & mechanics (MEMS)

Synchronous Circuits

- Controlled by global clock signals

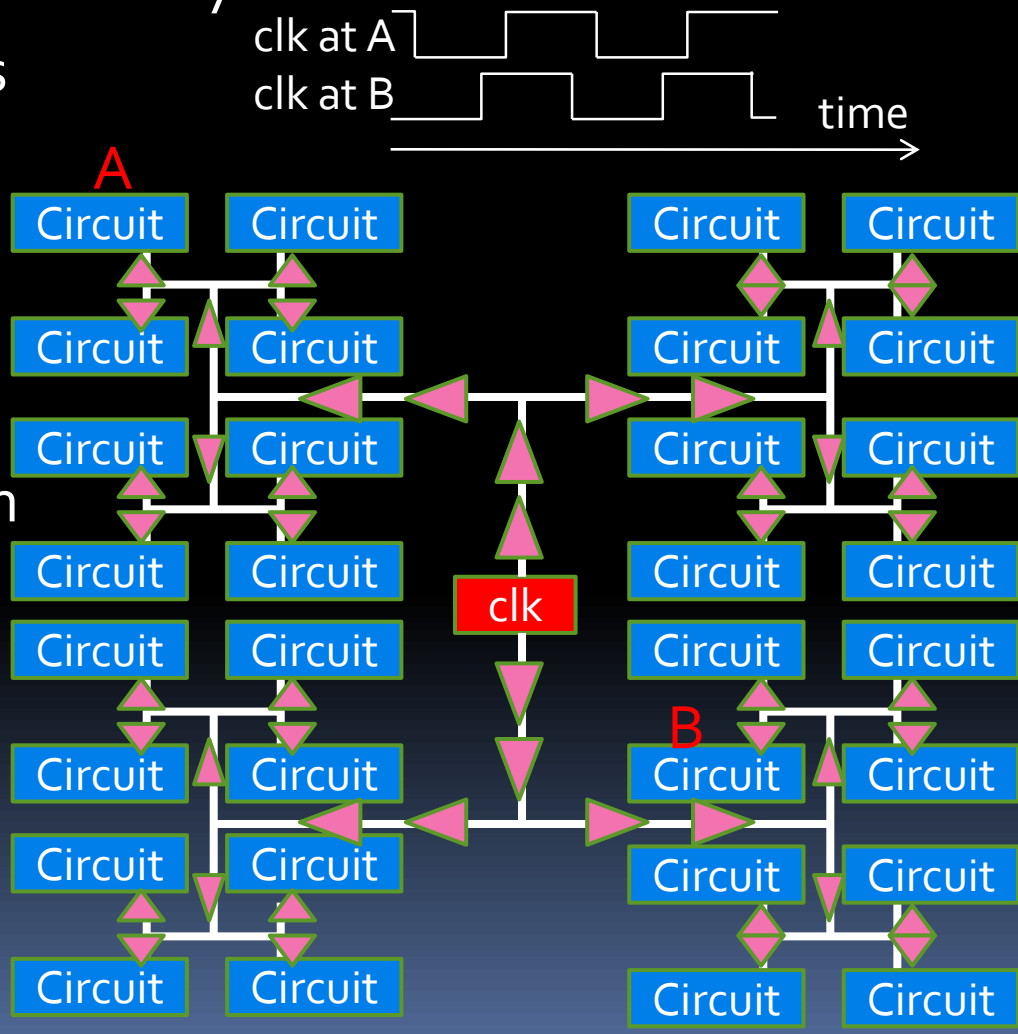




Problems on Synchronous Circuits

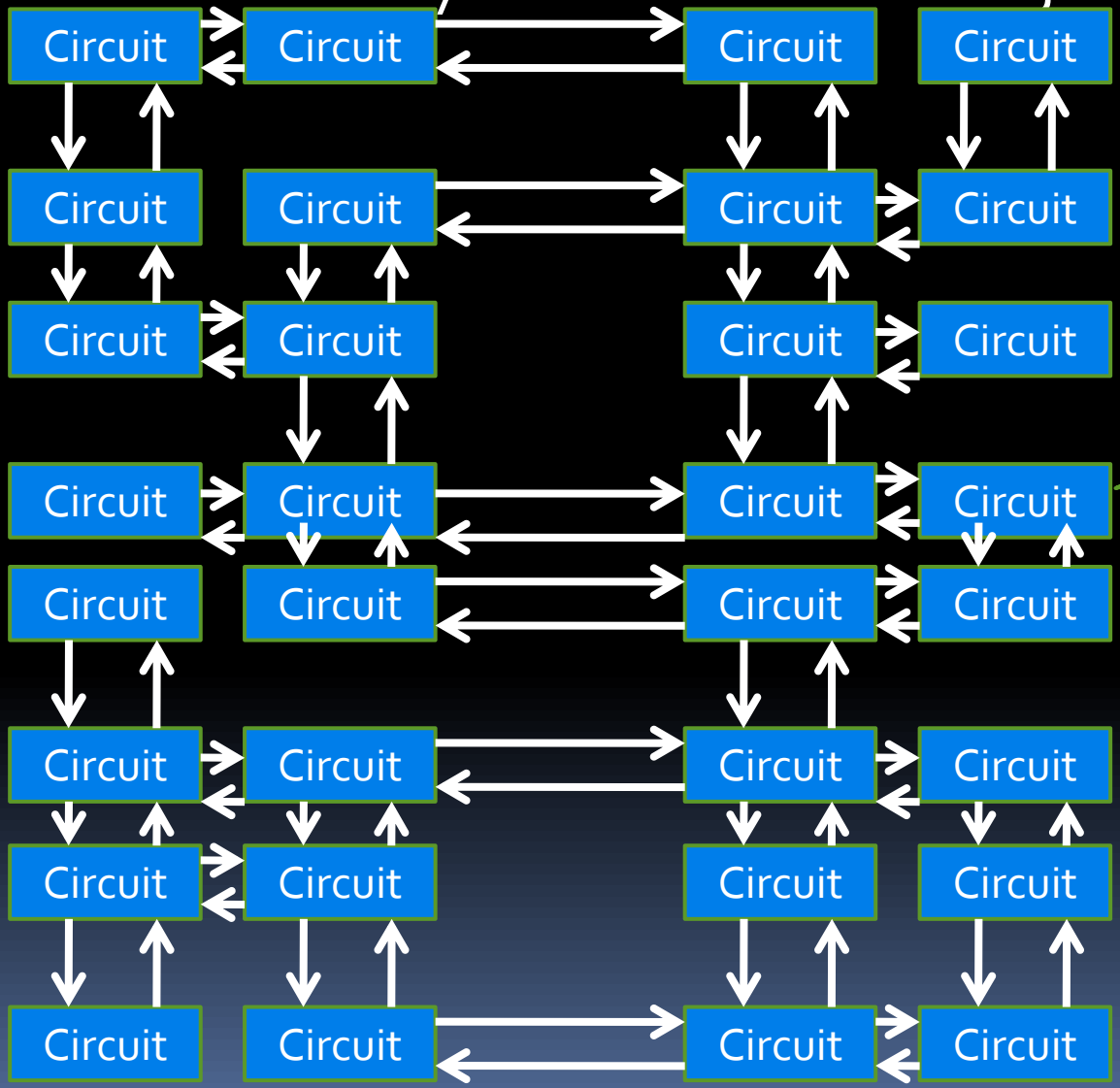
- Global clock network
  - Clock skew caused by wire delays
    - Synchronization failures
  - Large area
  - Power consumption
  - Large noise

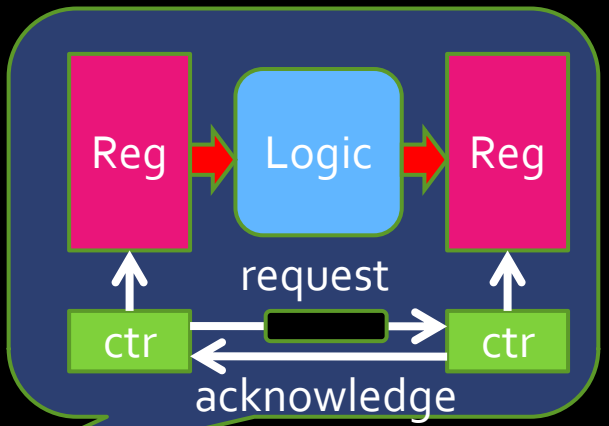
More and more significant when deep-submicron technology advances



Asynchronous Circuits

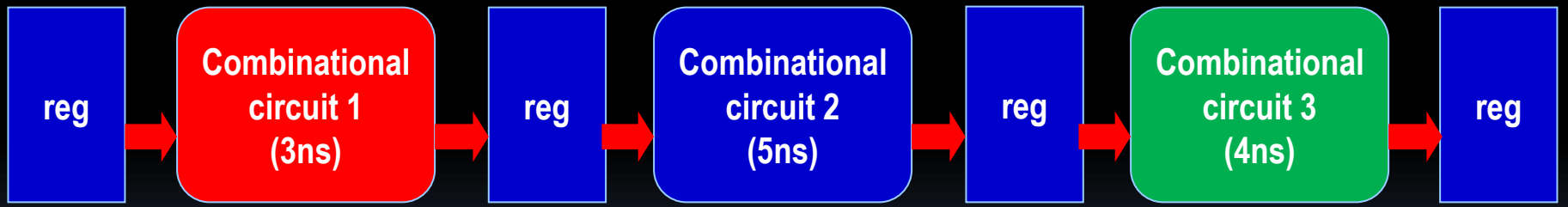
- Controlled by local handshake signals

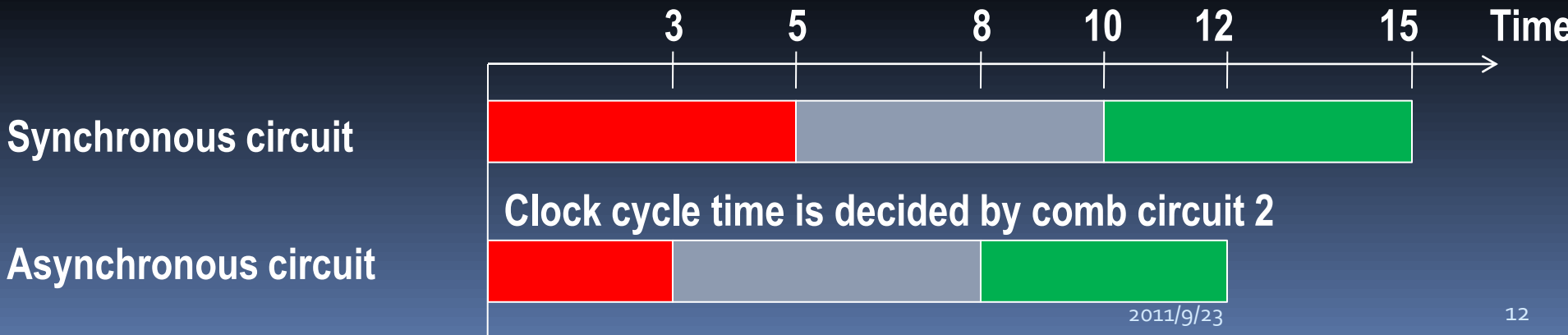




Advantages

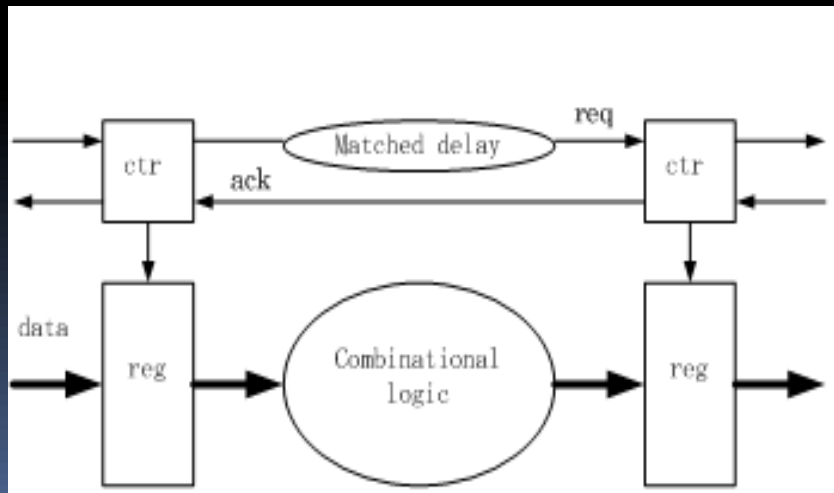
- No global clock signals
  - Low power
    - Operated only when required
  - Low electromagnetic interference
    - The execution of operations is distributed
  - High performance

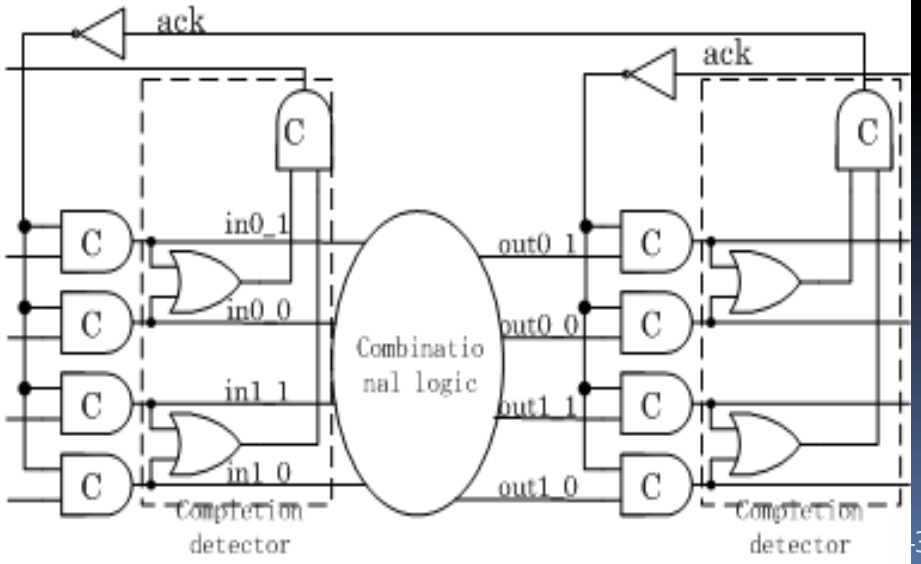




Implementation of Asynchronous Circuits

- Bundled-data implementation
  - Control timing is guaranteed by a delay element
    - Worst case delay
  - Less overhead
    - Data-path circuit used in the synchronous circuit can be used
- Two-rail implementation
  - Control timing is guaranteed by the completion detector
    - Average case performance
  - Large overhead



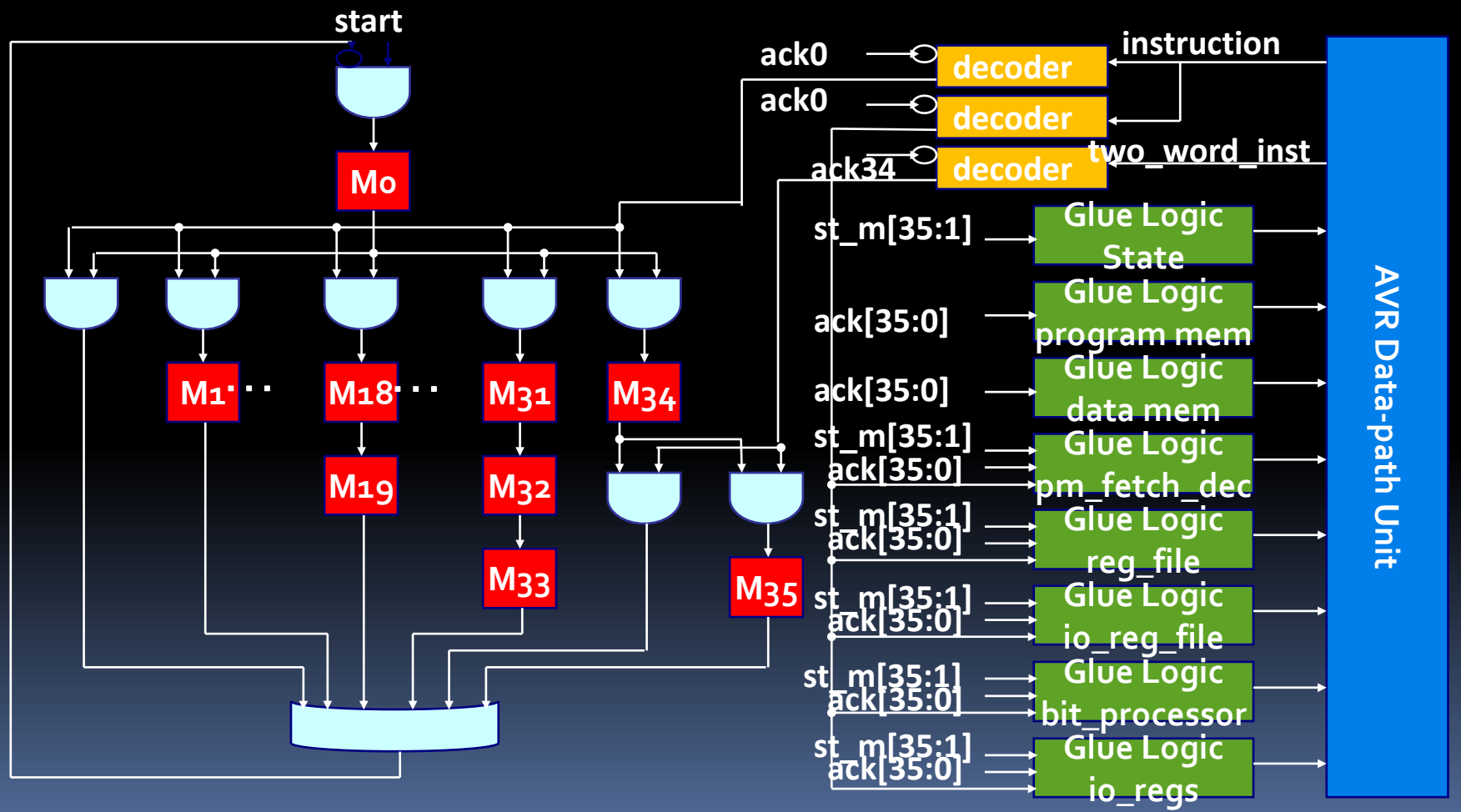


Perspective (from ITRS Roadmap)

- 2009 Edition, Design
  - GALS (Globally Asynchronous Locally Synchronous) for reliable communication (page 12)
    - To solve problems related to global wires
  - Automated handshake logic/circuit tools
    - Need for asynchronous and latency-insensitive global communication on chip (page 13)
  - Locally asynchronous designs for process variability (page 29)

Perspective (from Our Experiments)

- ATmega 103 (AVR processor)
  - 8bit microcontroller



Perspective (from Our Experiments)

- ATmega 103 (AVR processor)
  - 8bit microcontroller

ASIC Design with Rohm 0.18 um
The data are after layout synthesis

Benchmark		Synchronous AVR	Synchronous AVR (clock gating)	Asynchronous AVR	Asynchronous AVR (with opt)
EWF	Exec time	5,100 ns	5,100 ns	4,512 ns	4,319 ns
	Power	0.1028 W	0.0815 W	0.0470 W	0.0491 W
	Energy	524.28 nJ	415.65 nJ	212.064 nJ	212.0629 nJ
Isqrt	Exec time	3,396 ns	3,396 ns	3,011 ns	2,804 ns
	Power	0.1021 W	0.0791 W	0.0427 W	0.0464 W
	Energy	346.7316 nJ	268.6236 nJ	128.5697 nJ	130.1056 nJ
Icubrt	Exec time	6,828 ns	6,828 ns	5,960 ns	5,518 ns
	Power	0.1007 W	0.0785 W	0.0410 W	0.0449 W
	Energy	687.5796 nJ	535.998 nJ	244.36 nJ	247.7582 nJ
Crc32	Exec time	31,338 ns	31,338 ns	26,829 ns	25,061 ns
	Power	0.1037 W	0.0819 W	0.0458 W	0.0484 W
	Energy	3,249.7506 nJ	2,566.5822 nJ	1,228.7682 nJ	1,212.9524 nJ

Problems

- Difficult to design compared to synchronous circuits
  - Hazard-free implementation
  - Appropriate delay model, data encoding scheme, and control protocol should be selected
    - The design method and the design constraints are different according to the selection

Design automation is indispensable

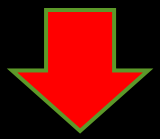
ITRS roadmap 2009 edition mentions:
by 2012, further progress in asynchronous clocking will depend on commercial tool support

Problems

- Overhead for handshake protocol
  - Area
  - Performance
  - Power consumption

Challenges

- Many design automation methods and tools have been developed



Why not succeed?

- Partial automation only
- Use of unfamiliar specification language
- Use of special components

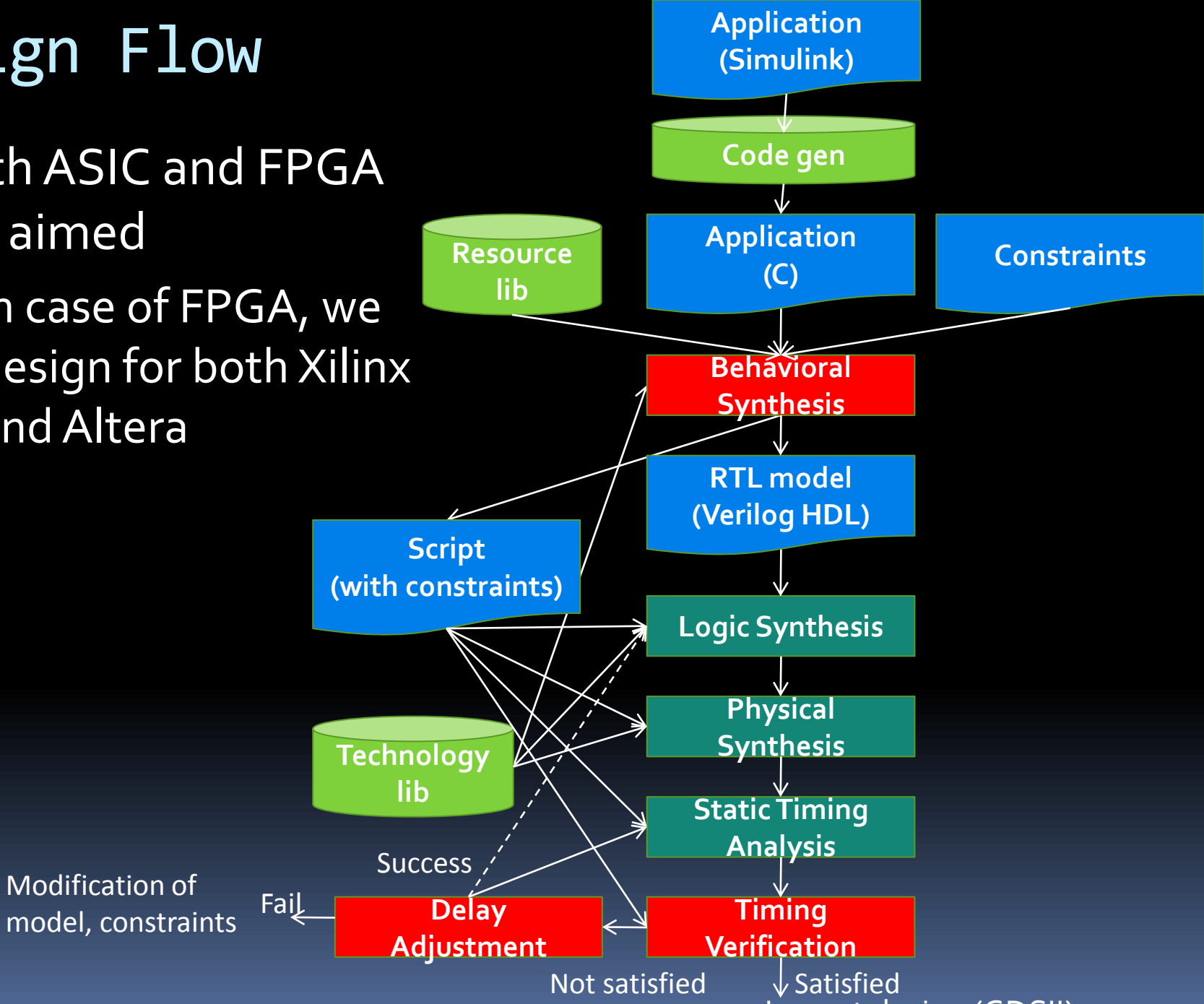
- Challenges
  - For automation
    - Use of commercial CAD tools
    - Only the part which is not supported by commercial CAD tools should be newly automated
  - Use of a standard specification language
  - Use of standard components
  - Reduction of overhead for handshake protocol

Purpose

- Development of design automation tools for asynchronous circuits using
  - Standard specification language
  - Commercial CAD tools
  - Standard components
- Optimization for handshake protocol
- Application of asynchronous circuits to real designs
  - For low power/low energy (e.g., portable systems)
  - For low electromagnetic radiation (e.g., systems with mixed signal)
- Targets are processors, ASICs, and FPGAs

Design Flow

- Both ASIC and FPGA are aimed
  - In case of FPGA, we design for both Xilinx and Altera



Our Development

- Behavioral synthesis tool
  - From C model to RTL model through operation scheduling, resource allocation, and control synthesis
  - Generation of a script file used for commercial CAD tools
- STA support tool
  - Timing verification tool
- ECO support tool
  - Delay adjustment tool

Future Direction for Design Automation of Asynchronous Circuits

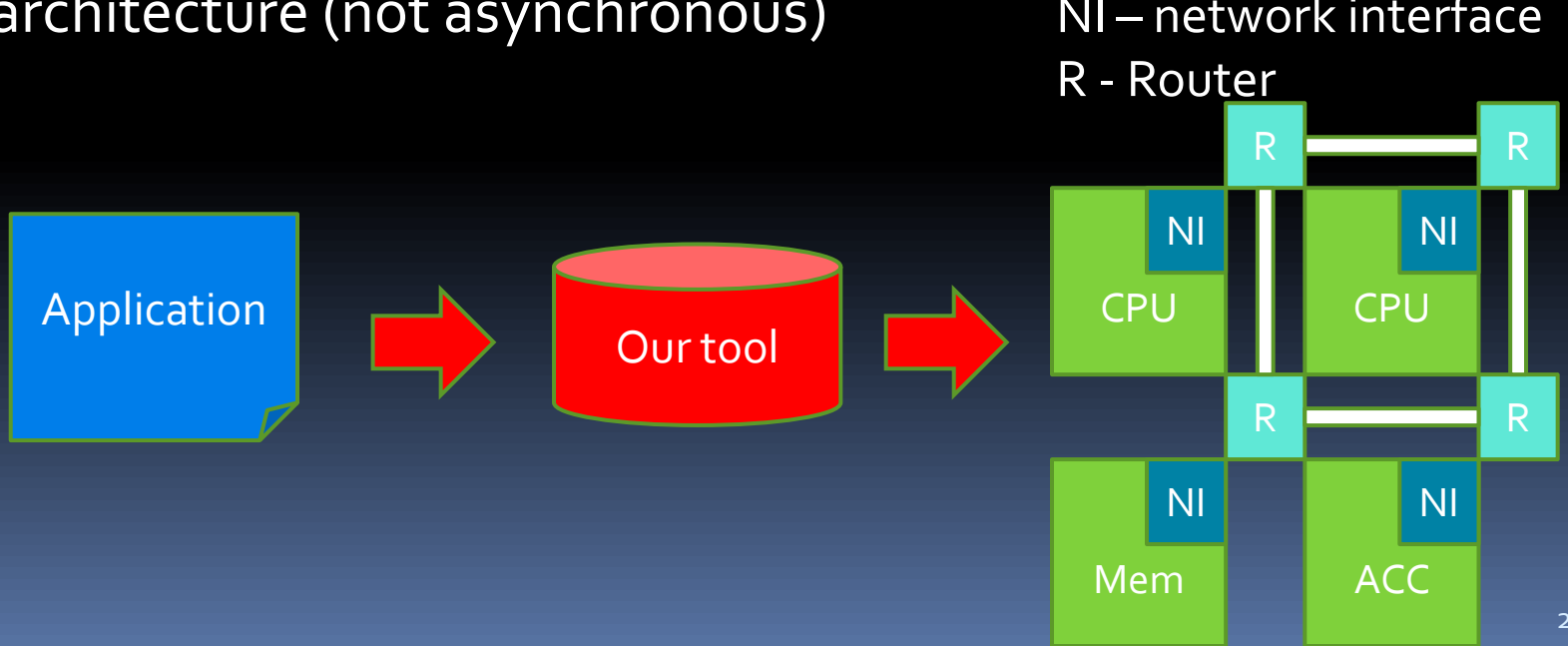
- Under development
  - Layout synthesis support tool
    - Floorplanner for performance optimization
  - Power optimization tool
- Within 3 – 5 years
  - Converter from synchronous circuits to asynchronous ones
  - Communication synthesis tool
    - To support communication with outside (e.g., synchronous circuits)
  - Verification tool
  - Support for testing

Our Activities (for Outside)

- Joint research with a Japanese company
  - Provided our developed CAD tool
  - Next step is to convert their product into asynchronous one
- Discussion with a Japanese company
  - Will provide the source code (Verilog HDL) of an asynchronous circuit

Our Activities (Funds)

- Grant-in-aid for scientific research (young scientist (B), H21-H23)
  - Energy optimization for asynchronous circuits
- Joint researches
  - A member of Dependable VLSI on JST/CREST (H21-H25)
    - Task allocation for dependable network-on-chip architecture (not asynchronous)



Long Term Plan

- Design of low power/low energy asynchronous circuits
  - Both general purpose and application specific
  - Tool distribution
- Development of CAD tools to support real system-level design
  - Hardware/software
  - Mixed signal

About Collaborations

- JSPS (Japan Society for the Promotion of Science)
  - Interchange between Japanese institute and other countries' institute
- Russia is included (Russian interface is Russian Foundation for Basic Research)
  - In case of 2012, 15 joint research proposals will be accepted (natural science is included)
    - 1 or 2 years
    - 2.5 million yen per year for Japanese institute (from JSPS)
    - 500,000 P per year for Russian institute (from RFBR)